Docket No.: 50006-128 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Makoto NAGATA, et al.	:	Confirmation Number: 4496
Serial No.: 09/977,994	:	Group Art Unit: 2857
Filed: October 17, 2001	:	Examiner: West, Jeffrey R

For: METHOD AND APPARATUS FOR ANALYZING A SOURCE CURRENT WAVEFORM IN A SEMICONDUCTOR INTEGRATED CIRCUIT

DECLARATION UNDER 37 CFR 1.132

Mail Stop Non-Fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, Makoto Nagata, hereby declare and say as follows:

1. That I am a joint inventor of the subject matter claimed in patent application Serial No. 09/977,994 (hereinafter the "`994 application").

2. That I and Mr. Atsushi Iwata, the named inventors, invented the subject matter claimed in the `994 application.

3. That I, Mr. Iwata, Mr. Jin Nagai, Mr. Katsumasa Hijikata and Mr. Takashi Morie are co-authors of the article entitled "Quantitative Characterization of Substrate Noise for Physical Design Guides in Digital Circuits" and published in the IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, March 2001.

4. That Mr. Nagai, Mr. Hijikata and Mr. Morie did not invent the subject matter claimed in the '994 application. Rather, they worked under my and Mr. Iwata's direction when co-authoring the subject matter claimed in the '994 patent.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

2004. 1. 21
Date

Makoto Nagata